Jeff Stevens

Pleasanton, CA 925-426-9170 (home) 925-980-1321 (cell)

I am fluent in most aspects of product development processes and medical design controls, including:

- Project management including scheduling, budget, team leadership, resource allocation
- Requirement definition, documentation, and flow down to subsystems
- Product risk management planning, execution, and documentation
- System architecture definition and documentation (block diagrams and text descriptions)
- Embedded control and user interface software architecture and coding using LabVIEW
- Structured alternative comparisons using trade-off analysis techniques
- External standard compliance, including electrical, physical and biological safety
- Verification and validation test planning, execution, and documentation
- Requirement management tools including DOORS, Requisite Pro, and RMTrak

Engineering Education

- **MSEE**, University of Colorado, 1990, 3.6 GPA
- **BSEE**, University of Wisconsin, 1985, 3.9 GPA

Professional Experience

Cabochon Aesthetics **Principal Engineer** **6/2008 – 5/2009**

- Wrote system and software requirements and verification procedures
- Defined and documented system architecture
- Selected and qualified all treatment cart components
- Built and tested prototype configurations
- Defined and arranged user interface controls and displays
- Wrote all software: closed loop machine control code, communications, logging and user interface
- Wrote code with National Instrument's (NI) LabVIEW Professional Development System
- Control code targeted Compact RIO hardware comprising large scale FPGA, real-time processor
- User interface code written for touch screen pc running embedded Windows XP
- Wrote additional code to automate component qualification and system performance lab tests

Sanarus **Principal System Engineer, then Project Manager** **11/2005 – 5/2008**

- Defined architecture for industry's first low pressure liquid nitrogen cryoablation system
- Wrote requirement, design description, and verification test documents
- Developed framework for, and lead system hazard analysis and FMEA
- Rewrote company's risk management process to comply with IEC 14971
- Executed trade off studies to select user interface and system control processing devices
- Recognized by CEO for key choice enabling 14 month development from requirements to revenue
- Defined control architecture, executed detail design and component selection/qualification
- Designed electronics and power distribution subsystems
- Selected software development environment and software architecture
- Mastered National Instruments LabVIEW, obviating outsourced software development
- Wrote all software: closed loop machine control code, communications, logging, user interface
- Wrote system technical description for 510(k) submission
- Executed and verified post launch software updates supporting new, smaller probe
- Managed project resulting in industry's smallest low pressure liquid nitrogen cryoablation probe
- Probe performed so well that target tumor size was expanded beyond the original requirement
- Praised for team morale improvement arising from open communication and team building skills

Jeff Stevens

Tyco – Puritan Bennett Principal System Engineer, then Senior Project Manager 11/2003 – 11/2005

- Managed $13M multi-year project to develop Puritan Bennett's first home care lung ventilator
- Responsible for budget, schedule, cost of goods, and product features and performance
- Directed 12-member core team plus a 35-member extended team representing all facets of medical device design and manufacturing
- Was Principal Systems Engineer for the project prior to taking over as Project Manager
- Wrote and maintained product requirements documents
- Define ventilator architecture and wrote system specification
- Lead system hazard analysis process, wrote document, lead subsystem FMEAs
- Ensured compliance with FDA guidelines and external safety standards
- Established DOORS requirement management scheme and maintained DOORS trace matrix
- Trained team on risk management requirements, fault tree analysis, FMEA process, and DOORS
- Recognized by 20-year Regulatory veteran as the best project manager in his experience

TheraSense Senior System Engineer 1/2001 – 11/2003

- Wrote system and subsystem requirement documents
- Lead architecture, features, and performance definition for Navigator continuous glucose monitor
- Conducted and documented system hazard analysis
- Coordinated verification testing process; wrote and conducted system level verification protocols
- Wrote system technical description for PMA submission
- Created user interface scheme and unique, flowchart-like diagram to describe it
- Selected, administered, and trained team on DOORS requirements management software tool
- Rewrote Risk Management Policy and Procedure to comply with ISO 14971

Tyco – Nellcor Senior System Engineer 1/1999 – 12/2000

- Defined and fulfilled role of System Engineer at Nellcor facility
- Wrote system and subsystem requirement documents
- Defined architecture, features, and performance of next generation OxiMax pulse oximeters
- Conducted system hazard analysis, ensured conformance to FDA recognized standards
- Designed Huffman-coded compression for storing saturation and heart rate on sensor

Integrated Device Technology DSP System Design Engineer 9/1997 – 12/1998

- Simulated IDT's first 155 Mbps ATM transmitter/receiver to use DSP techniques
- Preliminary digital algorithm verification was done using C++
- Block diagrams and end-to-end, bit-perfect simulation were done using MATLAB Simulink

Lattice Semiconductor Senior Product Planning Engineer 4/1996 – 9/1997

- Drove development of Lattice's then-next generation 5000-series CPLDs
- Specified architecture, performance, packaging and feature set
- Resolved conflicting requirements from hardware, software, and marketing
- Responsible for the development schedule through data sheet sign off

AMD/Siemens Field Application Engineer 9/1994 – 3/1996

- Penetrated new accounts to uncover design opportunities
- Guided designers to optimum solutions, and provided technical support

ESL Senior Engineer 4/1991 – 9/1994

- Drove 5-engineer team designing 120 Mbps, I/O board for massively parallel DSP computer
- The board, comprising 250 ICs including 3 Xilinx FPGA designs, 14 PAL designs, and a custom VME interface, went from concept to test in 4 months
- Defined board, VME, and FPGA blocks, designed several of the PALs, and debugged board
- Designed 1.25 Gbit/sec, GaAs 16-by-16 crosspoint switch for the same DSP computer

University of Colorado **Honorarium Instructor** **8/1990 – 3/1991**

- Developed and taught course in Boolean Algebra and Logic Design
- Refined ability to effectively communicate complicated concepts to the marginally interested

Hughes Aircraft **Member of Technical Staff, then Group Head** **7/1985 – 3/1991**

- Responsible for 5 engineers' task assignments, performance, development, and annual reviews
- Designed several ECL and GaAs systems running at clock rates from 200 MHz to 400 MHz
- Pioneered site's use of GaAs logic, surface mount, and high-speed multilayer circuit boards

Professional Achievements

- Runner up, Wall Street Journal's 2008 Technology Innovation Award, Medical category
- National Instruments Humanitarian of the Year award winner, 2008
- Finalist, National Instruments Graphical System Design Achievement Award, 2008
- Sole inventor for US Patents 6836721 and 7003393
- Spot cash awards totaling over $6400 from Tyco/Nellcor for shortening development time
- Published "A Digital Demodulator for Commercial FM Broadcast", 1990
- Selected for Hughes Aircraft MSEE Fellowship program
- Member of Tau Beta Pi, a National Engineering Honor Society
  Elected University of Wisconsin Chapter President
- Member of Phi Kappa Phi, a National Interdisciplinary Honor Society
- Member of Mensa, an International High IQ Society